AN171

Digital Filtering using the PDSP16256

Application Note

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INTRODUCTION

In the field of high performance filtering, engineering solutions are making increasing use of digital techniques. Digital filters are known to typically offer improved accuracy, complete predictability, flexibility and performance improvements. They are also highly suitable for integration with modern CAD tools and techniques, thus reducing development times and simplifying the design process.

General purpose DSP processors can implement digital filters with sampling rates upto approximately 250kHz, but until recently sampling rates beyond this threshold required complex custom design. However the latest CMOS design techniques now enable dedicated standard parts of the necessary speed and complexity to be fabricated, rendering custom designs obsolete.

WHAT ARE DIGITAL FILTERS?

'When a signal that is sampled in time and quantized in amplitude is processed such that the spectral characteristics of the signal are altered in a controlled manner then the resulting operation is termed digital filtering'.

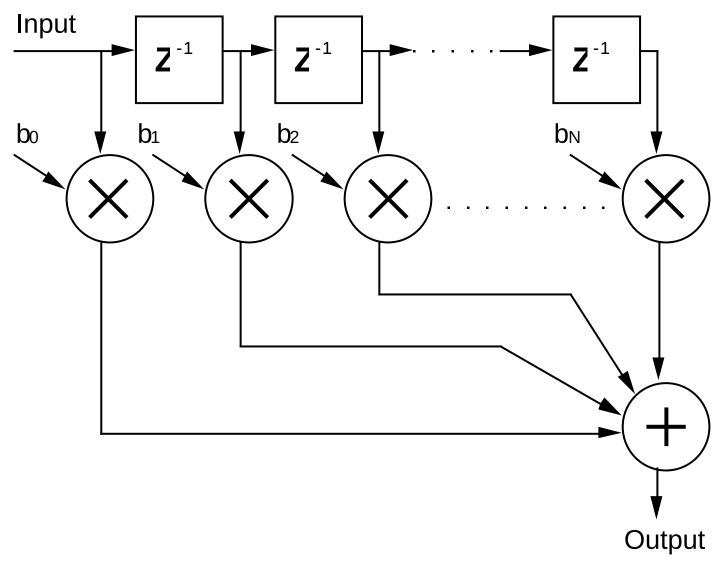

Fig 1 FIR Filter Structure.

Digital filters fall into two groups, those with infinite impulse response (IIR) and those with finite impulse response (FIR). The main difference between these two types is that the output from an FIR filter may be calculated from only current and previous inputs, whereas the output of an IIR filter depends on previous output states as well. Although IIR filters may be designed to be more efficient than an FIR for a given filter order, consideration must always be given to the stability of any design. FIR filters on the other hand, are inherently stable, are generally easier to design and implement in hardware and have the additional advantage that they may be designed such that they are free of phase distortion (i.e. constant group delay).

The output, y_n of an FIR may be calculated as the convolution of the input samples with the filter impulse response and can be represented by a difference equation such as:

$$y_n = b_0x_n+b_1x_{n-1}+.....+b_{N-1}x_{n-N+1}$$

or more generally:

$$y(n) = \sum_{k=0}^{N-1} h(k).x(n-k)$$

where coefficients b_k represent the N samples of the impulse response, h(k), of the desired filter.

WHAT IS THE PDSP16256?.

The PDSP16256 is a single chip FIR filter solution that is capable of operation at sample rates upto 25MHz. Internally it is arranged as two banks of eight multiplier/accumulators that are configurable in a number of ways. Each bank can be configured as a filter of 8, 16, 32, or 64 taps each doubling in length resulting in a halving of the maximum sample rate. The banks can be internally arranged as one single long filter, 2 independent filters, or 2 filters in connected in series. In addition a decimate option allows the output sample rate to be half the input sample rate, thus doubling the filter length. This mode ideal for low pass filter implementations since the high frequencys present in the input can be removed so the output still satisfies Nyquist's sampling criterion.

If the realization of the desired filter is beyond the capabilities of a single device then a number of devices in single filter mode can be cascaded to produce a filter with more taps, due to the provision at external pins of the full 32bit intermediate results.

DEVELOPMENT SYSTEM

A complete development system for the PDSP16256 is available from ERA Technology Ltd, consisting of a software package for filter design specifically tailored to the operating modes of the device and an IBM PC compatible board and control software.

The design package uses special procedures to quantize the filter coefficients in such a manner as to ensure an optimal filter response, given the internal bit accuracies. Low pass, high pass, Hilbert, delay, bandpass or bandstop filters are all supported. The user is given the option to leave any one of the filter design parameters free, and the software then determines this free parameter using the remaining specified parameters. Thus, for example, when designing a low pass filter the user can fix the number of taps to suit the maximum provided by the PDSP16256 at the required sampling rate. Either the transition band, pass band ripple, or stopband attenuation can then be left free, and the software will determine the best that can be achieved for that parameter, given the parameters which are fixed.

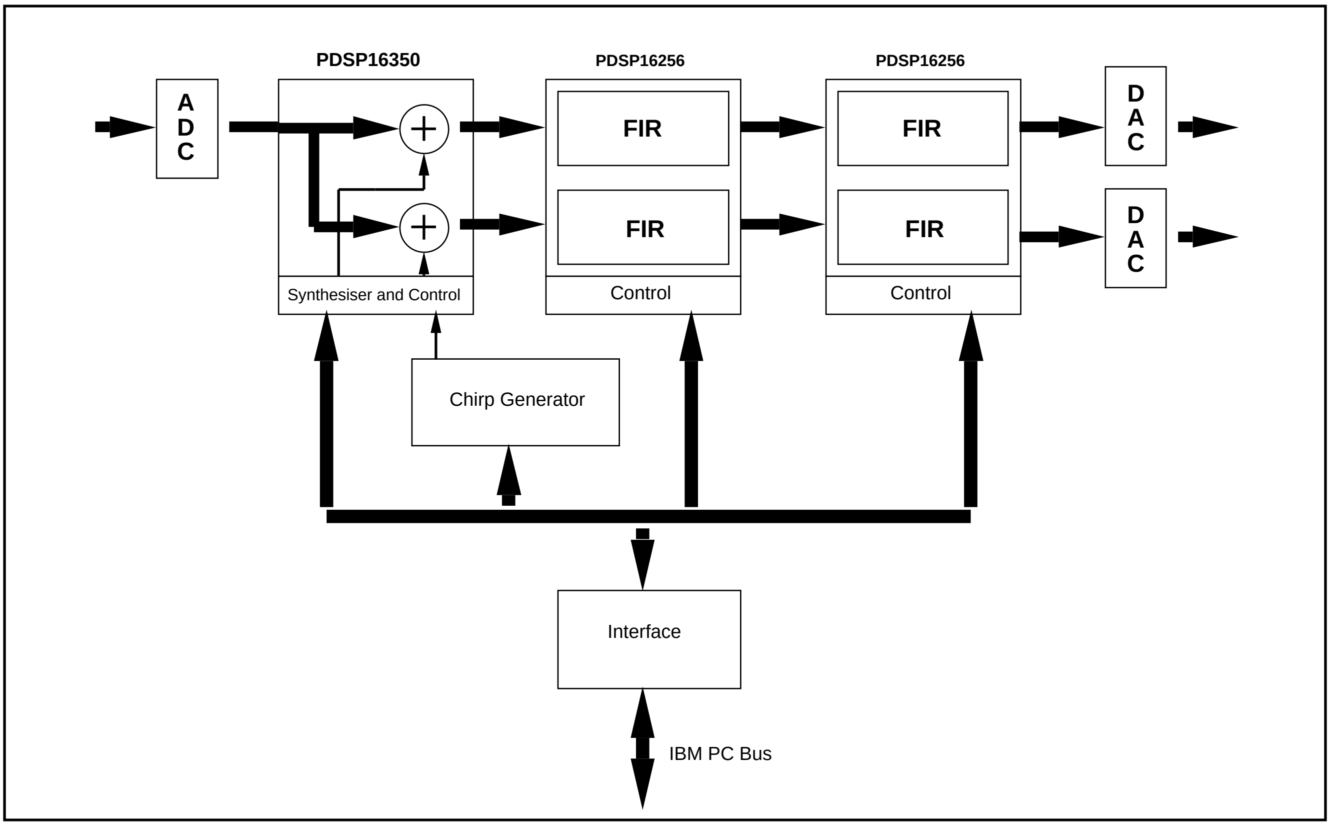

Fig 2 Schematic of Development Board.

The development board is arranged as shown in diagram 2. Digitization is undertaken using either a 20MHz eight bit ADC or a 1MHz twelve bit ADC. A quadrature mixing operation may be applied prior to filtering by means of a PDSP16350 I/Q splitter and numerically controlled oscillator. The digital filtering itself is undertaken using either one or two PDSP16256's. This configuration enables filters of upto 256 coefficients to be implemented using 16-bit data. It also provides the capability for cascaded filtering stages, or for two completely separate filters. The latter would be needed if the complex mixing option is in use. The output signal is available in digital form and in analogue form via dual 12-bit DAC's. The software supplied for the board controls configuration, enables loading of coefficients and can synthesize various waveforms.

EXAMPLES OF FILTERS IMPLEMENTED ON THE PDSP16256

The following filters are designed on the IBM PC design software and show in detail some of the performance characteristics achievable with the PDSP16256.

Figure 3 shows the frequency response of a 128 tap low pass filter designed for a cutoff frequency of 0.1 of the sampling frequency. As implemented on a single PDSP16256, configured in single filter, decimating mode, it exhibits a stop band rejection characteristic approaching -50dB.

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Fig 3 128 Tap Lowpass Filter on Single PDSP16256.

Figure 4 shows the frequency response of a filter designed to the same specification as the one shown in figure 3, but implemented as two 64 tap filters in series, again using a single PDSP16256.

It is clear that the series solution offers a much greater stop band rejection in practical applications but only as a trade off against the width of the transition band and at the expense of greater passband ripple.

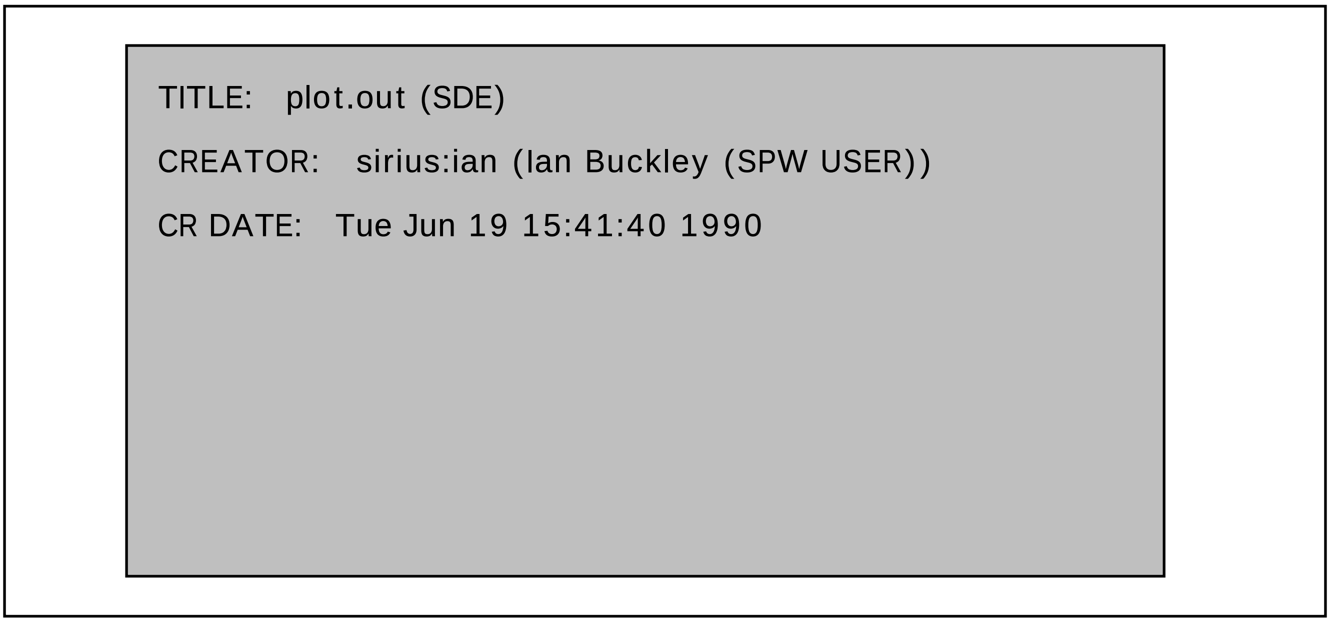

Fig 4 128 Tap Lowpass Filter Composed of two 64 Tap Filters in Series.

Figure 5 Illustrates the implementation of a narrow notch filter on a PDSP16256.

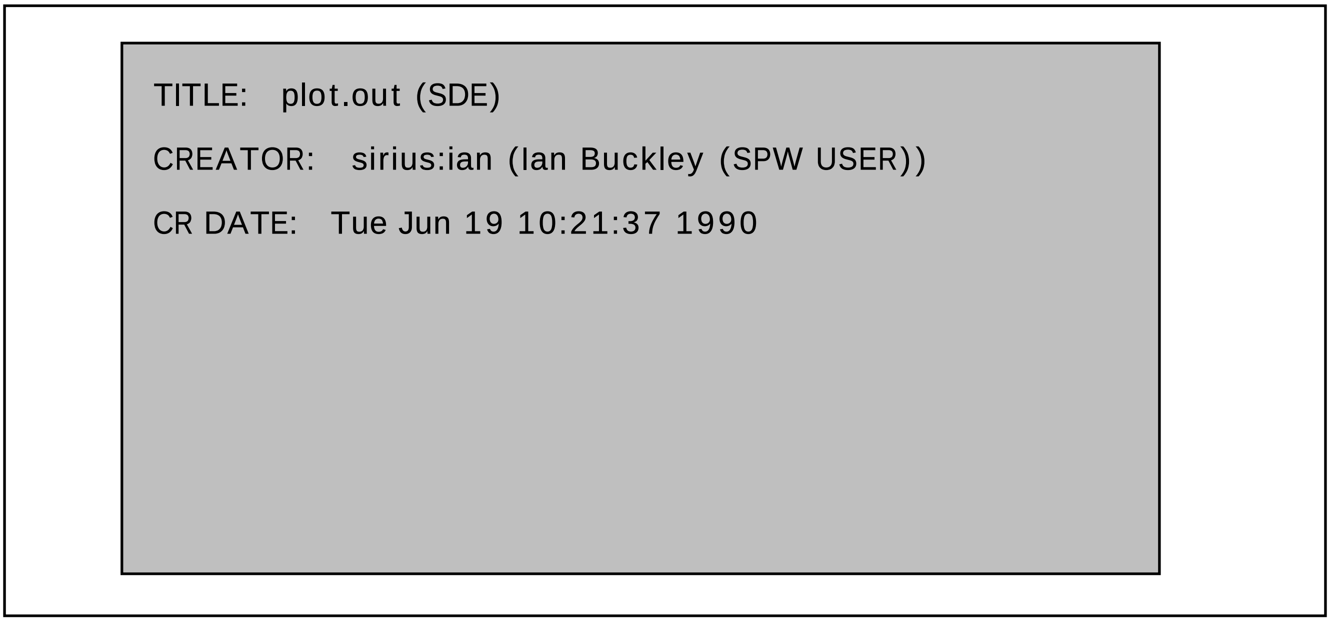

Fig 5 128 tap Bandstop Filter on a PDSP16256.

PRACTICAL SYSTEM CONFIGURATIONS

The PDSP16256 is designed with flexible interfacing characteristics to enable its use in a wide variety of system configurations. At it’s simplest it can be configured to auto load the filter coefficients directly from EPROM on power up and be directly connected to ADC's and DAC's (figure 6). Alternatively it could be configured as a dedicated co-processor for a general purpose programmable DSP processor with the DSP device controlling the PDSP16256 configuration, an architecture ideal for adaptive filtering applications for instance (figure 7).

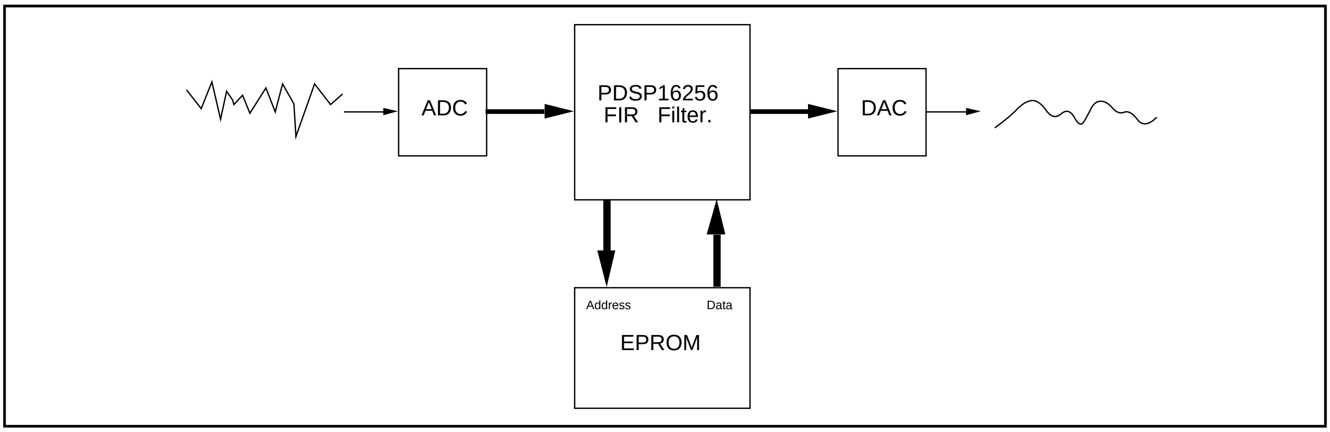

Figure 6 Simple Auto Load Configuration.

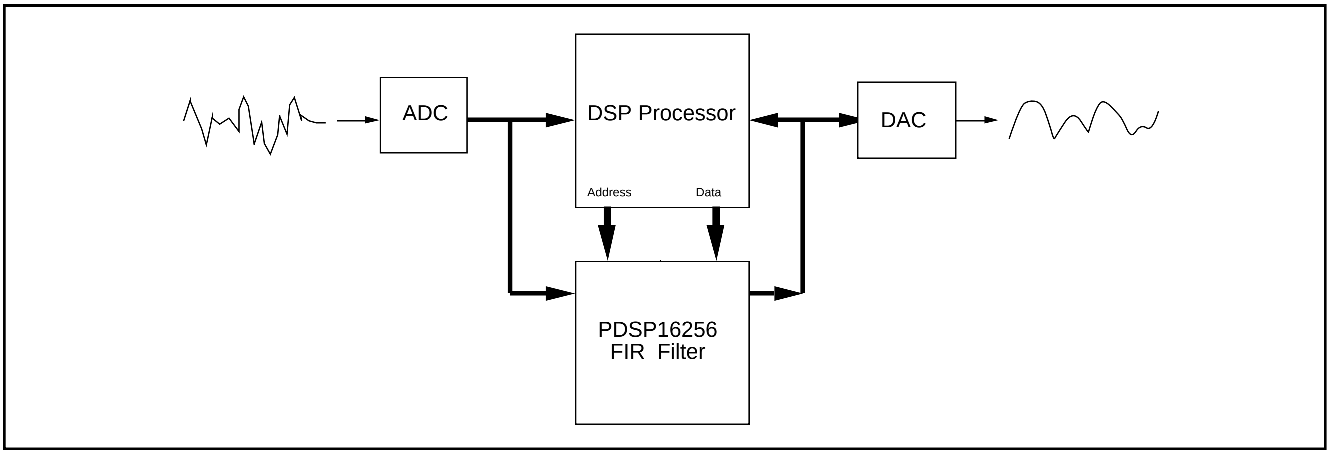

Figure 7 Slave Processor Configuration.

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